REMARKS

Claim 1 has been amended. No new matter has been added. Claims 1-6 are pending.

Disclaimers Relating to Claim Interpretation and Prosecution History Estoppel

Claim 1 has been amended, notwithstanding the belief that this claim was allowable. Except as specifically admitted below, no claim elements have been narrowed. Claim 1 has been amended solely for the purpose of expediting the patent application process, and the amendments were not necessary for patentability.

Any reference herein to "the invention" is intended to refer to the specific claim or claims being addressed herein. The claims of this application are intended to stand on their own and are not to be read in light of the prosecution history of any related or unrelated patent or patent application. Furthermore, no arguments in any prosecution history relate to any claim in this application, except for arguments specifically directed to the claim.

Claim Rejections - 35 USC § 103

The Examiner rejected claims 1-3 and 5 under 35 USC § 103 as obvious from van Rumpt (USP 6,922,550) in view of Patterson et al (UP 6,356,197). This rejection is respectfully traversed.

Van Rumpt discloses a communication device including a power amplifier for amplifying a modulated high frequency carrier input signal. The communication device comprises a resonance circuit and an excitation circuit. Setting the excitation duty cycle to be below 0.5 can realize a reduction of the signal power loss without affecting the amplifier output power.

Patterson discloses a tag comprising an LC circuit and a magnetic member connected in series to an inductor of the LC circuit. This is characterized in that a change in impedance of the magnetic member when exposed to an alternating magnetic field results in a change in the Q value of the resonance circuit.

Claim 1:

Claim 1 is independent. Claim 1 recites, among other features, "an amplitude of an output signal of said tuning circuit is varied by varying said resistance with said resistance-adjusting element based on the amplitude of the output signal of said tuning circuit." The Examiner asserted that van Rumpt teaches this feature at 7:11-40 and 4:28-36.

However, the resistance-adjusting element, as claimed, is a physically existing element like a transistor. Controlling the resistance-adjusting element based on the amplitude of the output signal of the tuning circuit causes its resistance when resonant to change and thus the amplitude of the output signal of the tuning circuit changes.

First, van Rumpt, at 7:11-12, discloses that resistor R represents the radiation resistance of the antenna means A. The radiation resistance is a virtual resistance that indicates the strength of radiation from the antenna means A, not a physically existing resistor. Also, the resistance of the resistor R is decided by the antenna means A. Accordingly, the resistance when resonant of the resonance circuit cannot be varied without changing the antenna means A. Also, even if assuming that the resistor R is a physically existing resistor, it is neither taught nor suggested that the resistance at time of resonance of the resonance circuit is varied by controlling the resistance of the resistor R.

Second, van Rumpt, at 7:25-41 and Fig. 1, discloses that the amplitude modulation means corresponds to a resonance circuit input means 2 and an amplitude modulator 5. The resonance signal amplitude varies according to the AM modulation signal because the excitation signal output from the resonance circuit input means 2 and the supply voltage from the amplitude modulator 5 both have been modulated in amplitude (van Rumpt, 10:2-5). In other words, the amplitude modulation means of van Rumpt does not vary the resistance at time of resonance of the resonance circuit 1 but varies the amplitude of the excitation signal and the supply voltage. Also, the amplitude modulation means does NOT perform control based on the amplitude of the output signal of the resonance circuit 1.

Third, Patterson, at 6:43-56, discloses that the variable resistive element is a magnetic member 12 connected in series to an inductor 8 of the LC circuit 3, wherein the magnetic member 12 changes its impedance when exposed to an alternating magnetic field, resulting in a change in the Q value of the LC circuit 3. As mentioned above, the magnetic member 12 is connected to the inductor 8 in series as claimed. Moreover, the magnetic member 12 does NOT perform control based on the amplitude of the output signal of the tuning circuit.

For at least the three reasons listed above, van Rumpt in view of Patterson does not render obvious claim 1.

Claims 2, 3 and 5:

By virtue of their dependence from claim 1, claims 2, 3 and 5 are not rendered obvious by van Rumpt in view of Patterson.

Claim 2 recites, among other features, "said resistance-adjusting element comprises a transistor, said resistance-adjusting element varying a voltage applied to a control electrode of said transistor in order to vary said resistance." The Examiner asserted that van Rumpt teaches this feature at 7:18-35.

However, van Rumpt, at 7:18-35, utilizes a parallel RLC circuit to excitate the resonance circuit. In contrast, as claimed, the resistance of the transistor is varied by turning the transistor ON/OFF based on the amplitude of the output signal of the tuning circuit. Thereby, the resistance at time of resonance of the tuning circuit is changed.

Since neither van Rumpt nor Patterson disclose or suggest the feature ""said resistance-adjusting element comprises a transistor, said resistance-adjusting element varying a voltage applied to a control electrode of said transistor in order to vary said resistance", van Rumpt in view of Patterson does not render obvious claim 2.

Claim 3 recites, among other features, "said resistance-adjusting element comprises a transistor, said resistance-adjusting element switching ON and OFF said transistor in order to vary said resistance." The Examiner asserted that van Rumpt discloses this feature at 7:18-35. More specifically, the Examiner asserted that the resistor R of van Rumpt comprises an inherent transistor corresponding to the transistor of the present invention.

However, as already mentioned, the resistor R represents the radiation resistance of the antenna means A. It is therefore impossible to interpret that the transistor R of van Rumpt comprises an inherent transistor. Also, even if assuming that the resistor R of van Rumpt is a physically existing resistor, it is neither disclosed nor suggested that the resistor R comprises a transistor and that the resistance at time of resonance varies by varying the voltage applied to the control electrode of the transistor or by turning the transistor ON/OFF.

Because neither van Rumpt nor Patterson teach or suggest the claimed feature, "said resistance-adjusting element comprises a transistor, said resistance-adjusting element switching ON and OFF said transistor in order to vary said resistance", van Rumpt in view of Patterson does not render obvious claim 3.

Claim 6:

The Examiner rejected claim 6 under 35 USC § 103 as obvious from van Rumpt (USP 6,922,550) in view of Patterson et al (UP 6,356,197) and further in view of Dykema et al (USP 5,699,055). This rejection is respectfully traversed.

Dykema et al. discloses a tuning circuit comprising an LC resonator. By virtue of its dependence from claim 1, claim 6 is not obvious from van Rumpt in view of Patterson. Nothing in Dykema overcomes the shortcomings of van Rumpt and Patterson. Therefore, claim 6 is not obvious from van Rumpt in view of Patterson and further in view of Dykema.

Claims 1-4:

The Examiner rejected claims 1-4 under 35 USC § 103 as obvious Morijiri et al (publication titled "A Wireless Communication System Suitable for Excessive Received Signal by Using New Damp Circuits) in view of Patterson et al (USP 6,356,197). This rejection is respectfully traversed.

Morijiri, published 01-24-2003, is not prior art with regard to claims 1-4, as priority is claimed to Japanese patent application number 2003-016147, a translated copy of which is attached. Therefore, Morijiri can not render obvious claims 1-4.

Thus, it is respectfully requested that the rejection be withdrawn.

Claim 5:

The Examiner rejected claim 5 under 35 USC § 103 as obvious in view of Morijiri et al (publication titled "A Wireless Communication System Suitable for Excessive Received Signal by Using New Damp Circuits) in view of Patterson et al (USP 6,356,197) and further in view of van Rumpt (USP 6,922,550). This rejection is respectfully traversed.

Morijiri, published 01-24-2003, is not prior art with regard to claim 5 as priority is claimed to Japanese patent application number 2003-016147, an unofficial translated copy of which is attached as Appendix A. Therefore, Morijiri can not render obvious claim 5.

Thus, it is respectfully requested that the rejection be withdrawn.

Claim 6:

The Examiner rejected claim 6 under 35 USC § 103 as obvious Morijiri et al (publication titled "A Wireless Communication System Suitable for Excessive Received Signal by Using New Damp Circuits) in view of Patterson et al (USP 6,356,197) and further in view of Dykema et al (USP 5,699,055). This rejection is respectfully traversed.

Morijiri, published 01-24-2003, is not prior art with regard to claim 6 as priority is claimed to Japanese patent application number 2003-016147, a translated copy of which is attached. Therefore, Morijiri can not render obvious claim 6.

Thus, it is respectfully requested that the rejection be withdrawn.

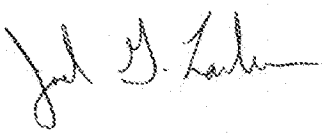
Conclusion

It is submitted, however, that the independent and dependent claims include other significant and substantial recitations which are not disclosed in the cited references. Thus, the claims are also patentable for additional reasons. However, for economy the additional grounds for patentability are not set forth here.

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is solicited. The Examiner is invited to call the undersigned attorney to answer any questions or to discuss steps necessary for placing the application in condition for allowance.

Respectfully submitted,

Date: July 14, 2006



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APPENDIX A

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

Date of Application: January 24, 2003

Application Number: Patent Application No. 2003-016147

Applicant(s): SANYO ELECTRIC CO., LTD.

March 25, 2004

Commissioner,
Patent Office

Yasuo IMAI (SEAL)

Certification No. 2004-302476

[NAME OF DOCUMENT] PATENT APPLICATION

[REFERENCE NUMBER] KGA1030005

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[CLASSIFICATION] H04L 27/02

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[AMOUNT] JPY 21,000

[LIST OF DOCUMENTS FILED]

[NAME OF DOCUMENT] SPECIFICATION 1

[NAME OF DOCUMENT] DRAWINGS 1

[NAME OF DOCUMENT] ABSTRACT 1

[PROOF] PROOF Required

[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] TUNING CIRCUIT HAVING AMPLITUDE-VARYING FUNCTION AND INTEGRATED CIRCUIT FOR WIRELESS COMMUNICATION DEVICE

[SCOPE OF CLAIM]

[Claim 1] A tuning circuit having an amplitude-varying function comprising:

a coil;

a capacitor; and

a resistance-adjusting element connected in parallel to said coil and said capacitor for varying resistance at time of resonance of said tuning circuit, wherein

an amplitude of an output signal of said tuning circuit is varied by varying said resistance with said resistance-adjusting element.

[Claim 2] The tuning circuit having an amplitude-varying function according to claim 1, wherein

said resistance-adjusting element comprises a transistor, said resistance-adjusting element varying a voltage applied to a control electrode of said transistor in order to vary said resistance.

[Claim 3] The tuning circuit having an amplitude-varying function according to claim 1 or 2, wherein

said resistance-adjusting element comprises a transistor, said resistance-adjusting element switching ON and OFF said transistor in order to vary said resistance.

[Claim 4] The tuning circuit having an amplitude-varying function according to claim 3, further comprising an automatic adjustment circuit system that includes:

a comparator that varies an output when said amplitude of

said output signal of said tuning circuit exceeds an automatic adjustment-use reference amplitude level; and

a transistor drive-use digital circuit that outputs, in response to said variance in said output of said comparator, a digital drive signal for varying said voltage applied to said control electrode of said transistor.

[Claim 5] The tuning circuit having an amplitude-varying function according to claim 1 to 4, wherein

a predetermined reference voltage is applied to respective ends of said coil and of said capacitor making up said tuning circuit, and wherein

an alternating current signal resonated by said tuning circuit is outputted from other ends of said coil and of said capacitor.

[Claim 6] The tuning circuit having an amplitude-varying function according to claim 1 to 4, wherein

respective ends of said coil and of said capacitor making up said tuning circuit are grounded, and wherein

an alternating current signal resonated by said tuning circuit is outputted from other ends of said coil and of said capacitor.

[Claim 7] An integrated circuit for a wireless communication device comprising said resistance-adjusting element and said automatic adjustment circuit system of the tuning circuit having an amplitude-varying function according to claim 4 to 6.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a tuning circuit having amplitude-varying function and to an integrated circuit for a wireless communication device.

[0002]

[Related Art]

A common example of a tuning circuit and an AGC (Automatic Gain Control) in, for example, ASK (Amplitude Shift Keying) communication is shown in Fig. 9. The tuning circuit is configured by an LC parallel resonance circuit where an end of a coil (inductance) L1 and a capacitor (capacity) C1 are connected to a reference voltage Vref. The AGC circuit is configured by a variable gain amplifier, a rectifying circuit (REC) and a comparator (COMP). The variable gain amplifier adjusts and outputs the amplitude of an AC signal from the tuning circuit to an output terminal OUT. A gain amplifier, a detecting circuit and a waveform shaping circuit are connected to the output terminal OUT, and the amplitude-adjusted AC signal is processed (e.g., see the Patent Document No.1).

[0003]

The gain factor of the AC (alternating current) signal in the variable gain amplifier is determined by the rectifying circuit and the comparator. That is, the amplitude of the AC signal is smoothed by the rectifying circuit to obtain a DC signal. Thereafter, the DC signal is compared with a reference voltage VAGC by the comparator. As a result of this comparison, the comparator feeds back output for lowering the gain factor to the gain amplifier in a case where, for example, the amplitude of the AC signal is excessive.

[0004]

The tuning circuit and the AGC circuit are used, for example,

in receiving devices of remote control systems. Remote control systems have various applications, such as opening/closing and locking the doors of vehicles and houses, and also starting and stopping engines in vehicles.

[0005]

[Patent Document No.1] Japanese Patent Application Laid-Open Publication No. Hei10-23084

[0006]

[Problem to be Solved by the Invention]

In realizing AGC functions such as, for example, conducting automatic control to lower the amplitude of an AGC signal in a case where the amplitude of the AGC signal is large, power consumption is great when an analog control system including the variable gain amplifier and the rectifying circuit is used. When a circuit that consumes a large amount of power is used in a battery-driven receiving device of a remote control system, battery drain is accelerated.

[0007]

[Means for Solving the Problem]

One aspect of the present invention is a tuning circuit having an amplitude-varying function comprising a coil, a capacitor, and a resistance-adjusting element connected in parallel to said coil and said capacitor for varying resistance at time of resonance of said tuning circuit, wherein an amplitude of an output signal of said tuning circuit is varied by varying said resistance with said resistance-adjusting element.

Thus, the amplitude of the output signal of the tuning circuit can be varied by varying the resistance of the tuning circuit with the resistance-adjusting element. Therefore, minute detection of the output signal is enabled by raising the

sensitivity of the tuning circuit and, even if the amplitude of the output and input becomes excessive, the amplitude thereof can be suppressed. That is, the invention can accommodate a wide dynamic range.

[0008]

The resistance-adjusting element can be comprised of a transistor and vary a voltage applied to a control electrode of the transistor in order to vary the resistance.

Thus, in varying the amplitude of the output signal of the tuning circuit, the resistance of the tuning circuit can be varied with an appropriate resistance of the transistor corresponding to the applied voltage.

[0009]

The resistance-adjusting element may be comprised of a transistor and switch ON and OFF the transistor in order to vary the resistance.

Thus, digital control becomes possible because the transistor that varies the resistance of the tuning circuit is switched ON and OFF. Thus, power consumption of the control system thereof can be reduced in comparison to a case where an analog control system is used. Especially in a case where the circuit of the invention is used in a battery-driven product, power consumption of a battery whose capacity is limited can be reduced.

[0010]

The tuning circuit having an amplitude-varying function of the present invention may further comprise an automatic adjustment circuit system, the automatic adjustment circuit system including a comparator that varies the output when the amplitude of the output signal of the tuning circuit exceeds an

automatic adjustment-use reference amplitude level, and a transistor drive-use digital circuit that outputs, in response to the variance in the output of the comparator, a digital drive signal for varying the voltage applied to the control electrode of the transistor.

Thus, the invention is disposed with the voltage-drivable automatic adjustment circuit system to realize the amplitude-varying function of the tuning circuit. As a result, power consumption can be significantly reduced in comparison to a case where a conventional analog control system is used. Power consumption of a battery whose capacity is limited can be reduced particularly in a case where the circuit of the invention is used in a battery-driven product.

[0011]

A predetermined reference voltage may be applied to one end of the coil and of the capacitor making up the tuning circuit, and the alternating current signal resonated by the tuning circuit may be outputted from the other ends of the coil and of the capacitor.

[0012]

One ends of the coil and of the capacitor making up the tuning circuit may be grounded, and the alternating current signal resonated by the tuning circuit may be outputted from the other ends of the coil and of the capacitor.

[0013]

An integrated circuit for a wireless communication device according to the present invention comprises the resistance-adjusting element and the automatic adjustment circuit system of the above-described tuning circuit having an amplitude-varying function.

[0014]

[Mode for Carrying Out the Invention]

===Principle===

Fig. 1 is a diagram showing the principle of a tuning circuit having an amplitude-varying function according to an embodiment of the invention. The tuning circuit is used, for example, in an antenna in a sending/receiving device of a communication system. As shown in the circuit diagrams of Fig. 1, a resistance-adjusting element R' is connected in parallel to a coil L1 and a capacitor C1 (top circuit diagram of Fig. 1) in an LC parallel resonance circuit configuring the tuning circuit. The resistance-adjusting element R' has a resistance (for convenience, this resistance will be referred to as R') by itself and varies a value (resistance) R0 of the resistance component at the time of resonance of the tuning circuit. A tuning circuit to which the resistance-adjusting element R' is not connected originally has a value of a resistance component R at the time of resonance (middle circuit diagram of Fig. 1). In addition, the resistance R0 of the tuning circuit to which the resistance-adjusting element R' is connected is represented by the inverse of (1/R + 1/R').

By varying the resistance R0 of the tuning circuit in this manner, a Q value of the tuning circuit is varied on the basis of the equation Q = R0/(□L1) (where □ is angular speed and L1 is the value of inductance of the coil L1). Due to the variance in the Q value, the level of the amplitude of the output signal of the tuning circuit can be varied. It should be noted that the Q value is selectivity representing the characteristics of the tuning circuit.

[0015]

Because the resistance R' of the resistance-adjusting element R' has a positive value, the resistance R0 of the tuning circuit to which the resistance-adjusting element R' is connected becomes smaller in comparison to the resistance R in the case where the resistance-adjusting element R' is not connected. As a result of the Q value becoming smaller in accompaniment with the resistance R0 of the tuning circuit becoming smaller, control that suppresses an excessive amplitude of an AC signal can be conducted.

[0016]

===Example===

An example of the circuit of Fig. 1 is shown in the circuit diagram of Fig. 2. The resistance-adjusting element R' of Fig. 1 is configured by a transistor MP0. In this example, the transistor MP0 is configured by a p-channel MOSFET. A reference voltage Vref (e.g., 3 V) is applied to one end (left side in the drawing) of a coil L1 and a capacitor C1 configuring the LC parallel resonance circuit that is the tuning circuit. An AC signal resonated by the LC parallel resonance circuit is outputted from an output terminal OUT (other end) of the coil L1 and of the capacitor C1.

[0017]

By varying the voltage applied to the gate (control electrode) of the transistor MP0, the resistance R0 of the tuning circuit is varied. In varying the voltage applied to the gate of the transistor MP0, there are the two arrangements of a digital drive arrangement that uses the transistor MP0 as a switching element and an analog drive arrangement that drives the transistor in an intermediate state between ON and OFF. For example, in a discrete analog drive arrangement, the voltage

applied to the transistor MP0 is set to a value in the range (e.g., 1V, 2V, 3V, etc.) of 0V (ON voltage) to 5V (OFF voltage). In so doing, plural discrete resistances are obtained between the drain and the source of the transistor MP0. Precise control of the amplitude levels of AC signals corresponding to these plural discrete resistances can be conducted.

[0018]

Next, description will be given of the digital drive arrangement that drives the transistor MP0 ON and OFF as a switching element. That is, the voltage applied to the gate of the transistor MP0 is set to 0V (ON voltage) or 5V (OFF voltage). For example, due to the transistor MP0 being switched ON, the resistance of the tuning circuit varies and the amplitude level of the AC signal from the output terminal OUT can be adjusted.

[0019]

Next, an example will be described, with reference to Fig. 3, where a tuning circuit having an AGC function is realized by adding an AGC circuit system (automatic adjustment circuit system) to the tuning circuit shown in Fig. 2. The AGC circuit system connected to the tuning circuit includes a level shift circuit ("Level Shift Circuit" in the drawing), a hysteresis comparator ("Hysteresis Comparator" in the drawing) and a transistor drive-use digital circuit.

[0020]

In the present invention, due to the principle of amplitude variance described with reference to Fig. 1, it is not necessary to use an analog circuit system of an adjusting circuit and variable gain amplifier such as in the conventional circuit shown in Fig. 9. For this reason, power consumption can be significantly reduced.

[0021]

First, description will be given in regard to the function of the AGC circuit system. The hysteresis comparator varies the output when the amplitude of the AC signal (output signal) from the tuning circuit becomes equal to or greater than a reference amplitude level for automatic adjustment. In accordance with the variance in the output of the hysteresis comparator, the transistor drive-use digital circuit outputs a digital drive signal VAGC for varying the voltage applied to the gate of the transistor MP0.

[0022]

In inputting the AC signal from the tuning circuit to the hysteresis comparator, the level shift circuit has the function of shifting the direct current level of the AC signal and making both the direct current levels consistent. That is, in the present example, a reference voltage Vref of 3V is applied to the tuning circuit. For this reason, when the transistor MP0 is switched ON and the resistance varies, an AC signal superposed on a direct current voltage of about 3V is outputted from the tuning circuit. The level shift circuit shifts the direct current component of about 3V from the tuning circuit to a direct current level sufficient for the hysteresis comparator to operate. Moreover, a central voltage of an automatic adjustment-use reference amplitude level serving as a comparative reference in the hysteresis comparator is also generated.

[0023]

Next, description will be given of a specific circuit configuration of the level shift circuit, the hysteresis comparator and the transistor drive-use digital circuit. First, the level shift circuit is configured by a level shift circuit

including a current mirror circuit. As shown in Fig. 3, the level shift circuit is configured by a level shifter section having an essential level shift function and a current mirror circuit section.

[0024]

The level shifter section is configured by a transistor (n-channel MOSFET) MN1, a transistor (n-channel MOSFET) MN2, a transistor (n-channel MOSFET) MN3 and a transistor (n-channel MOSFET) MN4. The AC signal from the tuning circuit is inputted to the gate of the transistor MN2. The drain and the source of the transistor MN4 are connected so that the transistor MN4 functions as a diode (resistance component).

[0025]

The current mirror circuit section is configured by a constant current source that supplies a constant current I1 and a transistor (n-channel MOSFET) MN5. The constant current I1 that the constant current source supplies serves as the source of the reference voltage (automatic adjustment-use reference amplitude level) applied to an inverted input terminal of the hysteresis comparator. The drain and the gate of the transistor MN5 are interconnected and also connected to the gate of the transistor MN3. The gate of the transistor MN3 is also connected to the gate of the transistor MN1 of the level shifter section, and the drain of the transistor MN3 is connected to the source of the transistor MN4. Also, both the transistor MN2 and the transistor MN4 are consistent and the direct current voltages of the sources of both are set to become equal. In the example circuit of Fig. 3, a direct current level that is lower than 3V by the gate-to-source voltage VGS of the transistor MN2 and the transistor MN4 is generated in the sources of the transistor MN2

and the transistor MN4.

[0026]

In the level shift circuit of this configuration, the source of the transistor MN2 is connected to a non-inverted input terminal (+) of the hysteresis comparator, and the source of the transistor MN4 is connected to an inverted input terminal (-) of the hysteresis comparator. Thus, a mutually equal 3V-VGS direct current voltage is applied to both the non-inverted input terminal and the inverted input terminal of the hysteresis comparator. That is, only a direct current is applied to the inverted input terminal of the hysteresis comparator, and the hysteresis comparator has a reference voltage (automatic adjustment-use reference amplitude level) at a high side and a low side of this direct current level. A signal whose direct current level has been level-shifted to 3V-VGS in regard to the AC signal from the tuning circuit is inputted to the non-inverted input terminal of the hysteresis comparator. That is, the hysteresis comparator compares the amplitude of the AC signal with the reference voltage and varies the output from "L" to "H" when the amplitude of the AC signal exceeds the reference voltage. The output of the hysteresis comparator is outputted to the transistor drive-use digital circuit.

[0027]

The transistor drive-use digital circuit outputs, in accordance with the variance in the output of the hysteresis comparator, a digital drive signal for varying the voltage applied to the gate of the transistor MN0. The transistor drive-use digital circuit is a voltage-driven circuit and includes a reset D flip-flop circuit FD2, an RSFF (set reset flip-flop) circuit configured by two NOR circuits NR1 and NR2,

and a NAND circuit ND1.

[0028]

The output of the hysteresis comparator is applied to a clock terminal C of the D flip-flop circuit FD2. With respect to the D flip-flop circuit FD2, a power supply VCC is connected to a data terminal D and an input terminal (reset terminal) of the NOR circuit NR1 is connected to an output terminal Q. Moreover, a reset terminal RESET is connected to a reset terminal RN of the D flip-flop circuit. The reset terminal RESET is also inversely connected to an input terminal of the NAND circuit ND1. With respect to the NAND circuit ND1, the power supply VCC is connected to the other input terminal, and the output terminal is connected to an input terminal (set terminal) of the NOR circuit NR2 of the RSFF circuit. Also, other alternatives exhibiting an inverter function are applicable for the NAND circuit ND1. It should be noted that, as is well known, the RSFF circuit has a basic configuration using the two NOR circuits NR1 and NR2. The digital drive signal VAGC is outputted from the output terminal of the NOR circuit NR1. Also, the RSFF circuit may be a reset D flip-flop circuit.

[0029]

The AGC operation will be described, with reference to the waveform chart shown in Fig. 4, with focus on the transistor drive-use digital circuit of this configuration. First, the point in time to a time T0 in Fig. 4—that is, the state of each signal in a state (reset state) where the level-shifted AC signal from the tuning circuit has not been inputted to the hysteresis comparator—will be described. The output of the hysteresis comparator (waveform "C" in Figs. 3 and 4), the output of the D flip-flop circuit FD2 (waveform "Q" in Figs. 3 and 4) and the

output of the NAND circuit ND1 ("waveform of the NAND circuit ND1" in Figs. 3 and 4) are in "L" states. The output of the NOR circuit NR1 (digital drive signal VAGC; waveform "VAGC" in Figs. 3 and 4) and the voltage applied to the reset terminal RESET (waveform "RESET" in Figs. 3 and 4) are in "H" states.

[0030]

A case will be described where from the point in time following the time T0 in Fig. 4, the AC signal is level-shifted and inputted from the tuning circuit to the hysteresis comparator, and the amplitude of this AC signal is excessive. After the AC signal having the excessive amplitude is inputted to the hysteresis comparator, the input level to the non-inverted input terminal becomes larger than the reference voltage to the inverted input terminal within the first several ms (time T0 to T1), whereby the hysteresis comparator varies the output C from "L" to "H". When this happens, the output Q of the D flip-flop circuit FD2 is switched to the "H" state, the RSFF circuit is reset and the digital drive signal VAGC is also inverted to the "L" state. As a result, the transistor MP0 is switched ON and, as described previously, the AGC with respect to the tuning circuit operates so that the amplitude of the AC signal is suppressed.

[0031]

It should be noted that the voltage applied to the reset terminal RESET is maintained in the "H" state. Thus, the "L" state of the digital drive signal VAGC is maintained in the "L" state and the ON state of the transistor MP0, which is the resistance-adjusting element, can be maintained (held) so that the AGC operation can be prevented from stopping.

[0032]

Thereafter, in a case where the AGC operation is stopped and the signal state of each section is initialized, an "L" reset-use pulse signal is applied to the reset terminal RESET (time T2). When this happens, the output Q of the D flip-flop circuit FD2 returns to the "L" state. At the same time, the output of the NAND circuit ND1 outputs an "H" pulse signal to match the reset-use pulse signal. The RSFF circuit is set to match the rise of this pulse signal and the digital drive signal VAGC is also inverted and switched to the "H" state. As a result, the transistor MP0 is switched OFF and, as described previously, the AGC operation with respect to the tuning circuit stops.

[0033]

Also, the reset D flip-flop circuit is applicable with respect to the RSFF circuit of Fig. 3 and the same operation can be obtained using the output thereof as the VAGC.

[0034]

===Another Modified Example===

A modified example of the embodiment that was described with reference to Figs. 1 to 4 is shown in Figs. 5 and 6 and will be described. That is, as shown in Fig. 5, the resistance-adjusting element R' is configured by the transistor MN0 comprising an n-channel MOSFET. An end (left side in the drawing) of the coil L1 and the capacitor C1 configuring the LC parallel resonance circuit that is the tuning circuit is grounded (GND connection). The AC signal resonated by the LC parallel resonance circuit is outputted from the output terminal (other end) of the coil L1 and the capacitor C1.

[0035]

Due to a modification wherein the n-channel MOSFET transistor MN0 is employed as the resistance-adjusting element

R' and the ends of the coil L1 and the capacitor C1 are grounded, the level shifter section of the level shift circuit is configured by a transistor (p-channel MOSFET) MP1, a transistor (p-channel MOSFET) MP2, a transistor (p-channel MOSFET) MP3 and a transistor (p-channel MOSFET) MP4, as shown in Fig. 6. The current mirror circuit section is configured by a constant current source supplying a constant current I1 and a transistor (p-channel MOSFET) MP5. The drain and the gate of the transistor MP5 are interconnected and also connected to the gates of the transistors MP1 and MP3. Thus, both the MP2 and the MP4 are consistent, whereby the direct current voltages of both are set to become equal. In the example circuit of Fig. 6, a direct current level that is higher than the GND by the gate-to-source voltage VGS of the MP2 and MP4 is generated in the sources of the MP2 and MP4.

[0036]

Also, the connection arrangement of the RSFF circuit outputting the digital drive signal VAGC is changed in comparison to the case of Fig. 3. The RSFF circuit has a well known basic configuration and connection state. That is, in Fig. 6, an input terminal of the NOR circuit NR1 of the RSFF circuit is connected to the output terminal of the NAND circuit ND1, and an input terminal of the NOR circuit NR2 of the RSFF circuit is connected to the Q terminal of the D flip-flop circuit FD2. In other words, when the output Q of the D flip-flop circuit FD2 becomes "H", the RSFF circuit is set and the digital drive signal VAGC of the "H" state is outputted.

[0037]

The operation of the circuit shown in Fig. 6 is the same as in the case of Fig. 3. That is, the AC signal resonated by

the tuning circuit is transferred to the hysteresis comparator by the level shift circuit. When the amplitude level of the AC signal becomes excessive and exceeds the reference voltage (automatic adjustment-use reference amplitude level), the output of the hysteresis comparator is varied from "L" to "H". As a result, the digital drive signal VAGC from the RSFF circuit is varied from "L" to "H", the transistor MN0 is switched to the ON state and the AGC operation begins.

It should be noted that, in a case where the AGC operation is stopped and the signal states of each section are initialized, the state of the signal applied to the reset terminal RESET is varied from "H" to "L".

[0038]

Here, a specific example of the aforementioned discrete analog drive will be described. In Figs. 3 and 6, plural values of, for example, 1V, 2V and 3V are set with respect to the voltages (drive signal VAGC) applied to the transistors MP0 and MN0. That is, in Figs. 3 and 6, they are connected in parallel to plural level hysteresis comparators CMP1, CMP2 and CMP3, and RS flip-flop circuits RSFF1, RSFF2 and RSFF3 are connected in correspondence to the hysteresis comparators CMP1 to CMP3, so that a plural level configuration is formed. The output terminals of the RS flip-flop circuits RSFF1 to RSFF3 are connected to a decoder. The drive signal VAGC is outputted from the decoder.

[0039]

A reference voltage Vref1 for generating the drive signal VAGC is set in an inverted input terminal of the hysteresis comparator CMP1. A reference voltage Vref2 for generating a 2V drive signal VAGC is set in an inverted input terminal of the

hysteresis comparator CMP2. A reference voltage Vref3 for generating a 1V drive signal VAGC is set in an inverted input terminal of the hysteresis comparator CMP3.

[0040]

The output from the level shift circuit ("Level Shift Circuit" in the drawing) is applied to non-inverted input terminals of the hysteresis comparators CMP1 to CMP3, and the results in which they are compared with the reference voltages Vref1 to Vref3 are outputted. 3-bit data (4 values: HHH, HHL, HLL, LLL) of the RS flip-flop circuits RSFF1 to RSFF3 are outputted to the decoder in accordance with the outputs of the hysteresis comparators CMP1 to CMP3. The decoder generates a uniquely determined drive signal VAGC (one of 1V, 2V and 3V) in accordance with the 3-bit data and outputs the drive signal VAGC to the transistors MP0 and MN0.

[0041]

Also, the reset D flip-flop circuit is applicable with respect to the RSFF circuit of Fig. 6 and the same operation can be obtained using the output thereof as the VAGC.

[0042]

===Example Applied to Remote Control System===

An applied example of the tuning circuit having an amplitude-varying function described in the preceding embodiment and modified example will be described with reference to Fig. 8. In this applied example, the invention is applied to, for example, a key 100 and a wireless door lock (or an engine starting and stopping) remote control system (two-way communication keyless system) for a vehicle 200.

[0043]

The key 100 is disposed with a receiving-use antenna

section 110, an RF (Radio Frequency) IC (Integrated Circuit) 120 that is an integrated circuit for a wireless communication device, a microcomputer 130, and a transmitting-use antenna section 140 configured by an LC oscillator circuit. The receiving-use antenna 110 is a tuning circuit disposed with the coil L1 and the capacitor C1 in Figs. 3 and 6 according to the invention. The RIFC 120 is disposed with the AGC circuit system in Figs. 3 and 6 according to the invention and the AGC including the transistors MP0 and MN0. In addition, the RFIC 120 is disposed, as is well known, with an amplifier AMP that amplifies the AC signal from the AGC, a detecting circuit DET, a comparator COMP and a flip-flop FF. The microcomputer 130 processes the output signal from the flip-flop FF. The microcomputer 130 also executes ASK transmission or FSK (Frequency Shift Keying) transmission through the transmitting-use antenna section 140 from a data output terminal DATA OUT of the microcomputer 130.

[0044]

The vehicle 200 is configured by a receiving-use antenna 210, an RFIC 220, a microcomputer 230 and a transmitting-use antenna section 240. Each of the constituent elements 210 to 240 is similarly configured by the receiving-use antenna section 110, the RFIC 120, the microcomputer 130 and the transmitting-use antenna section 140 of the key 100, and executes communication with the key 100.

[0045]

===Other===

Equivalents such as alternative circuits having the same function as that of the resistance-adjusting element of the invention are also included in the technical scope of the invention.

[0046]

[Effect of the Invention]

The amplitude of the output signal of the tuning circuit is varied by varying the resistance of the tuning circuit with the resistance-adjusting element. Therefore, minute detection of the output signal is enabled by raising the sensitivity of the tuning circuit and, even if the amplitude of the output and input becomes excessive, the amplitude thereof can be suppressed. That is, the invention can accommodate a wide dynamic range.

[0047]

Thus, in a case where the invention is disposed with a voltage-drivable automatic adjustment circuit system to realize the amplitude-varying function of the tuning circuit, power consumption can be significantly reduced in comparison to a case where a conventional analog control system is used. Power consumption of a battery whose capacity is limited can be reduced particularly in a case where the circuit of the invention is used in a battery-driven product.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

This is a diagram for contrasting, with a conventional tuning circuit, the principle of a tuning circuit having an amplitude-varying function according to an embodiment of the invention;

[Fig. 2]

This is a circuit diagram of the tuning circuit having an amplitude-varying function according to the embodiment of the invention;

[Fig. 3]

This is a circuit diagram of a tuning circuit having an

AGC function according to the embodiment of the invention;

[Fig. 4]

This is a waveform chart showing the state of signals of respective sections of a transistor drive-use digital circuit shown in Fig. 3;

[Fig. 5]

This is a diagram showing the principle of a modified example according to the embodiment of the invention;

[Fig. 6]

This is a circuit diagram showing a modified example of the tuning circuit having an amplitude-varying function according to the embodiment of the invention;

[Fig. 7]

This is a partial circuit diagram in a case where the tuning circuit having an amplitude-varying function according to the embodiment of the invention takes an analog drive arrangement;

[Fig. 8]

This is a block diagram showing an example where the tuning circuit having an amplitude-varying function according to the embodiment of the invention is applied to a wireless door lock remote control system of a vehicle; and

[Fig. 9]

This is a circuit diagram showing a conventional tuning circuit having an amplitude-varying function.

[DESCRIPTION OF REFERENCE CHARACTERS]

100 Key

110 Receiving-use antenna section

120 RFIC (Integrated circuit for wireless communication device)

123 Detecting circuit DET

130 Microcomputer

140 Transmitting-use antenna section

200 Vehicle

210 Receiving-use antenna

220 RFIC (Integrated circuit for wireless communication device)

230 Microcomputer

240 Transmitting-use antenna section

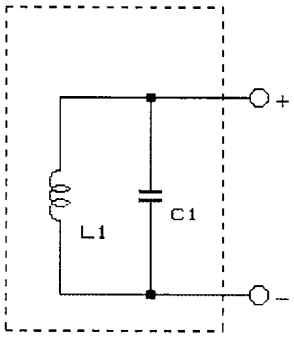
AMP Amplifier

COMP Comparator

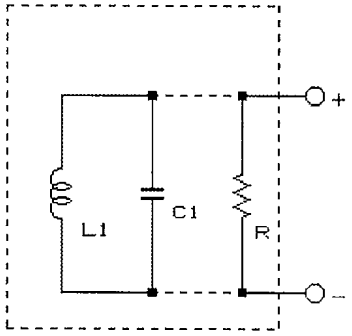
FF Flip-flop

[NAME OF DOCUMENT] DRAWINGS
[FIG. 1]

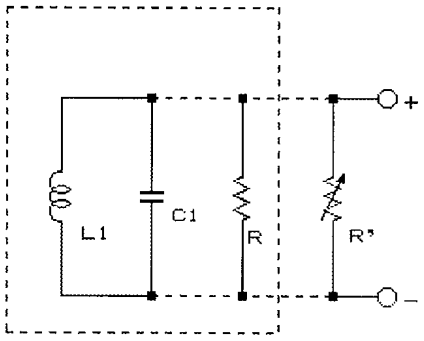
TUNING CIRCUIT



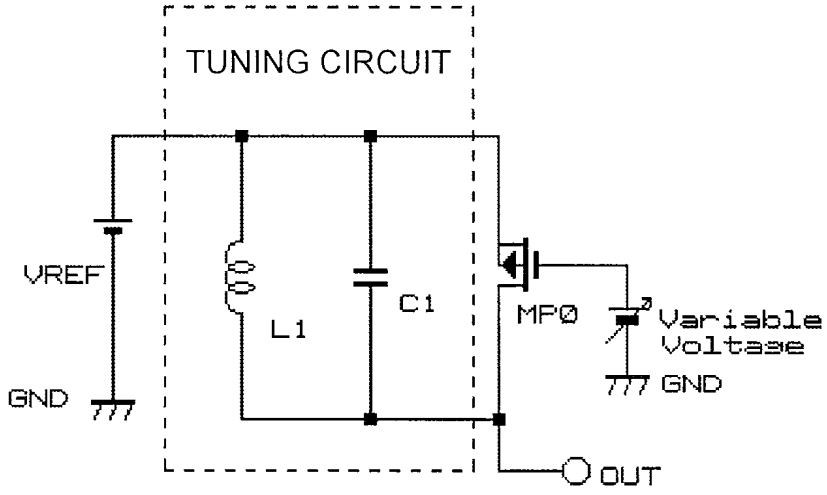
TUNING CIRCUIT



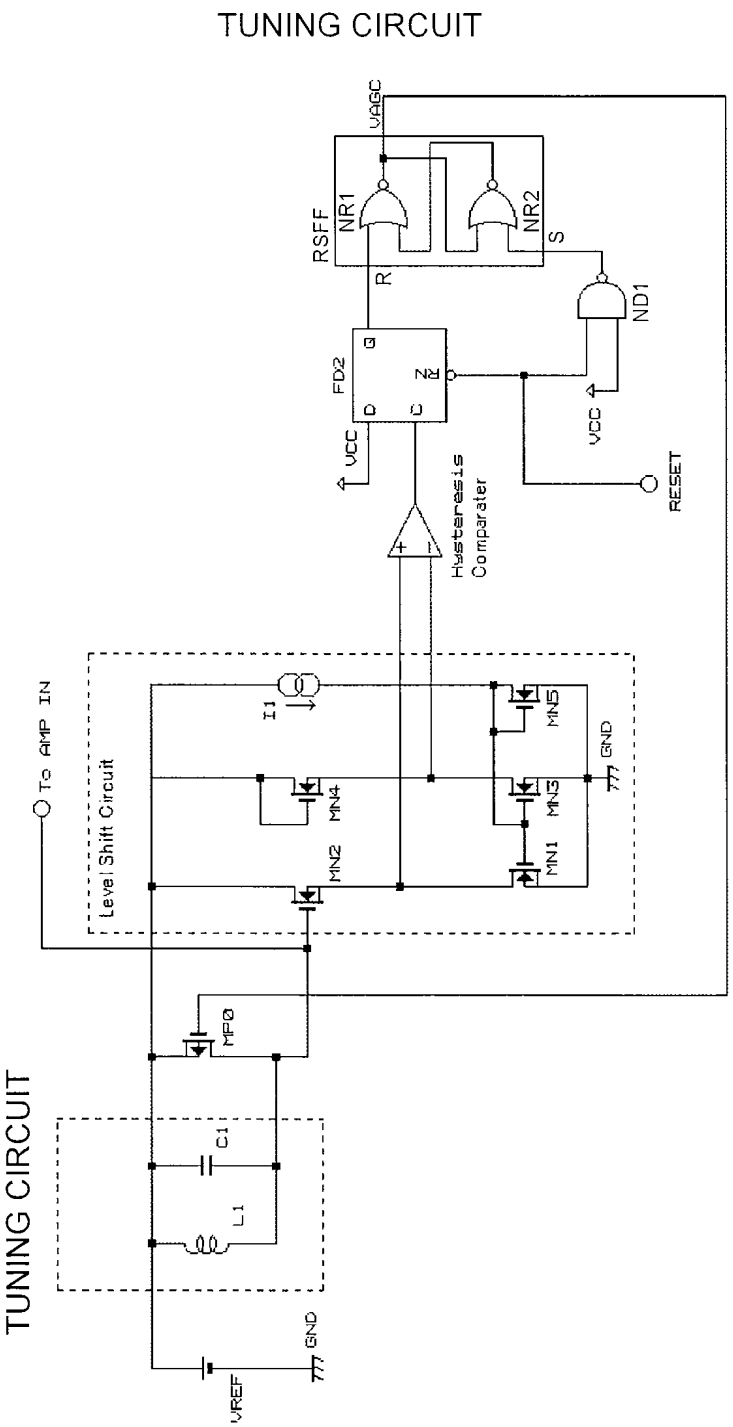
TUNING CIRCUIT



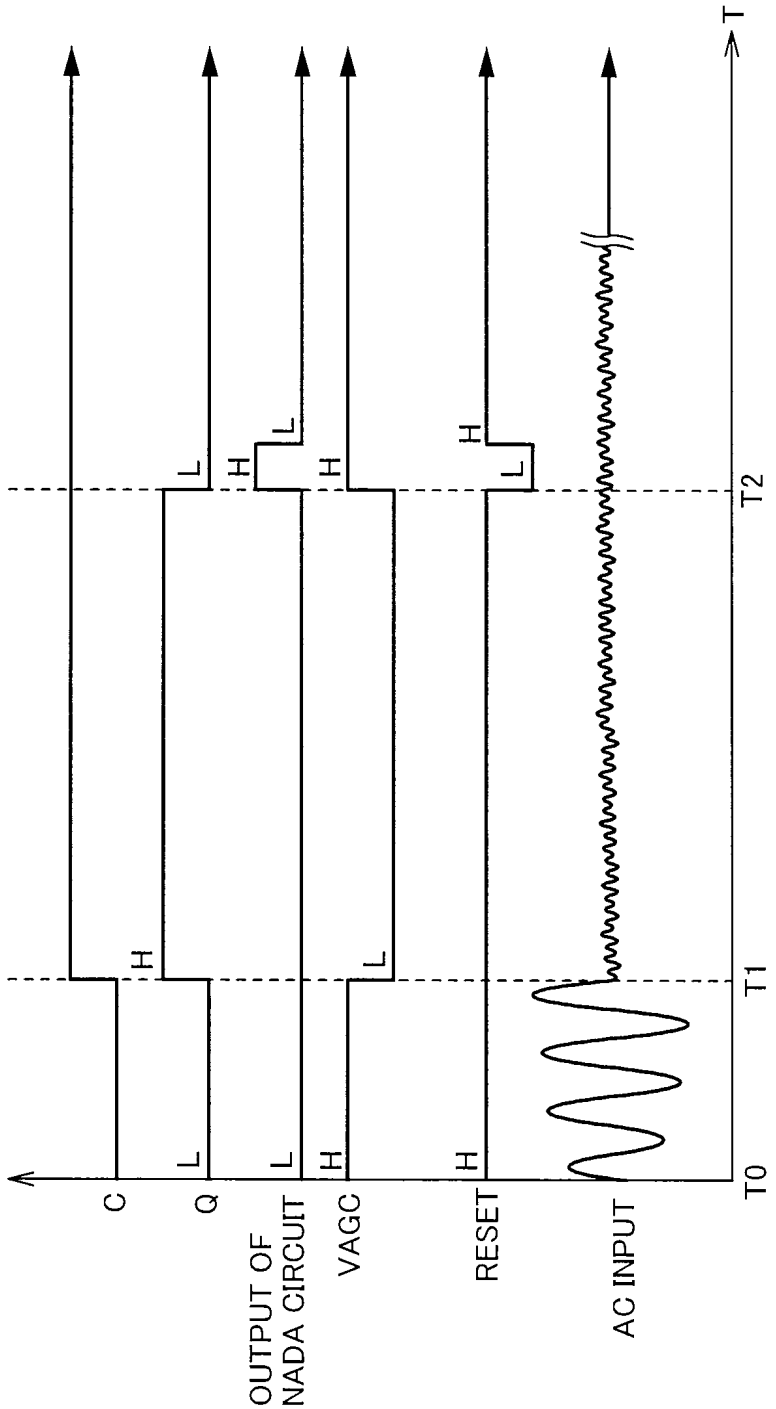
[FIG. 2]



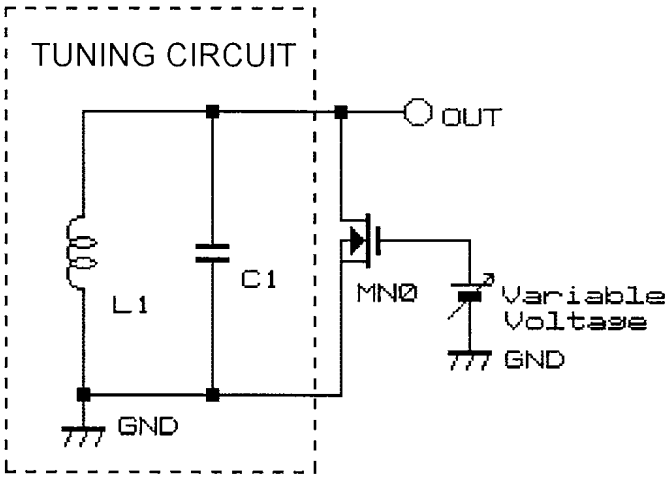
[FIG. 3]


TUNING CIRCUIT
VAGC
RSFF
NR1
NR2
S
R
ND1
FD2
Q
D
C
VCC
VCC
RESET
Hysteresis Comparator
To AMP IN
Level Shift Circuit
I1
MN5
MN4
MN3
MN2
MN1
GND
MP0
C1
L1
VREF
GND
TUNING CIRCUIT

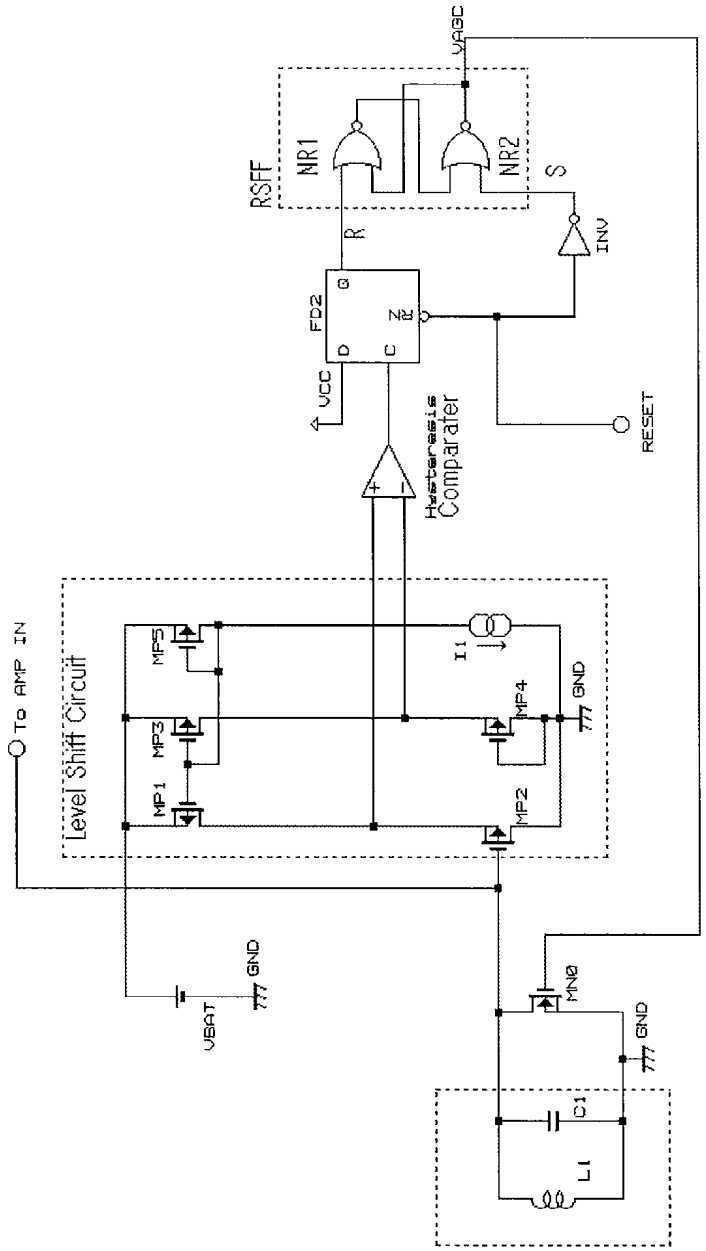
[FIG. 4]



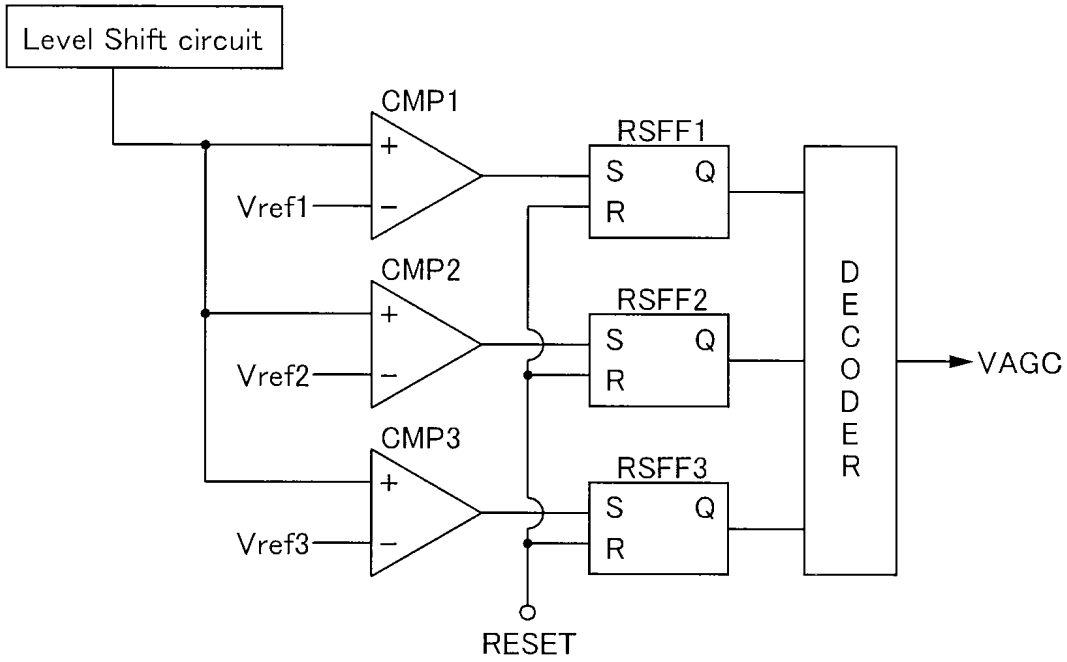
[FIG. 5]



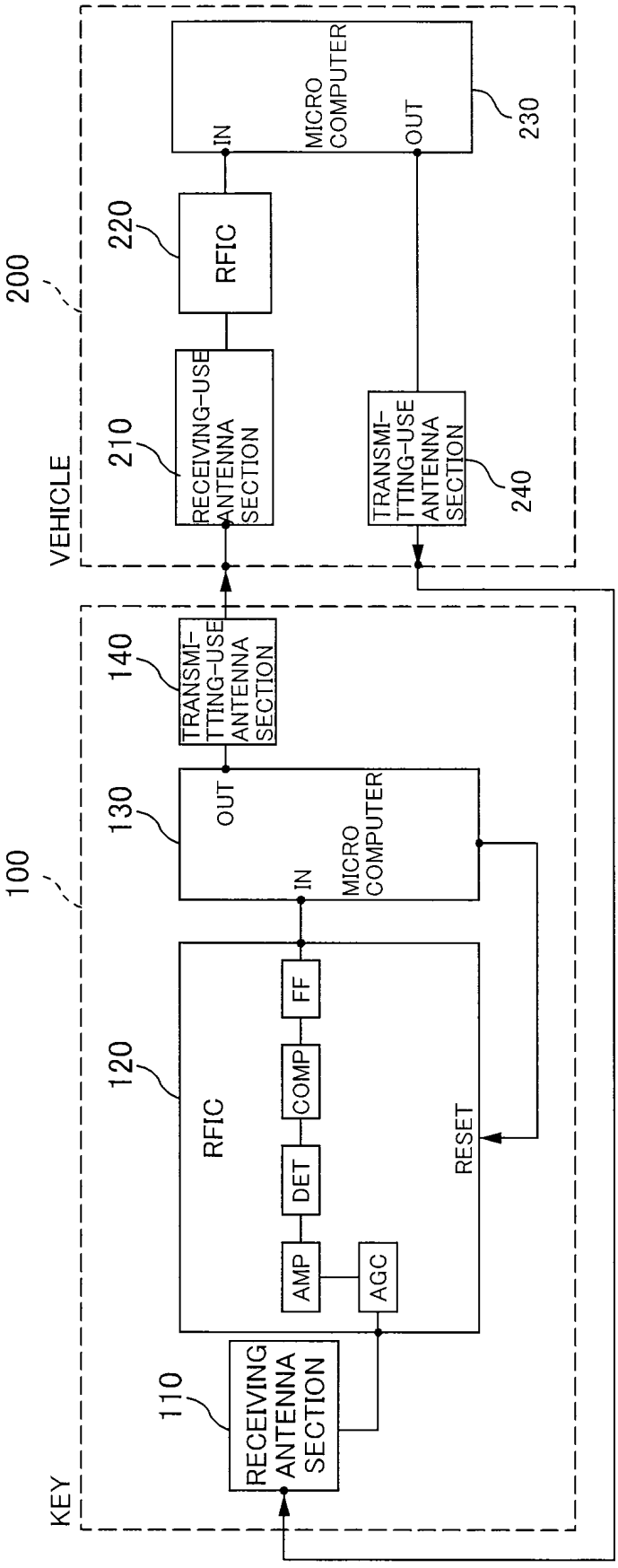
[FIG. 6]


VABC
RSFF
NR1
NR2
S
R
INV
FD2
Q
D
C
VCC
RESET
Hysteresis Comparater
To AMP IN
Level Shift Circuit
MP5
MP3
MP1
I1
MP4
MP2
GND
VBAT
MN0
C1
L1

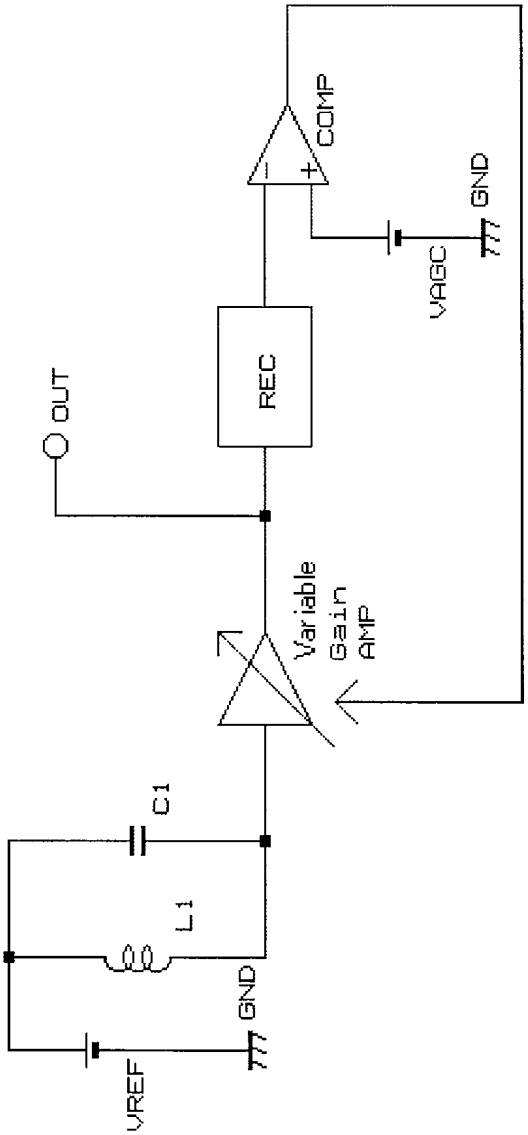
[FIG. 7]


Level Shift circuit
CMP1
CMP2
CMP3
Vref1
Vref2
Vref3
+
−
RSFF1
RSFF2
RSFF3
S
R
Q
DECODER
VAGC
RESET

[FIG. 8]


VEHICLE
200
MICRO COMPUTER
IN
OUT
230
220
RFIC
210
RECEIVING-USE ANTENNA SECTION
TRANSMI-TTING-USE ANTENNA SECTION
240
KEY
100
140
TRANSMI-TTING-USE ANTENNA SECTION
130
OUT
MICRO COMPUTER
IN
120
RFIC
FF
COMP
DET
AMP
AGC
RESET
110
RECEIVING ANTENNA SECTION

[FIG. 9]



[Name of Document] Abstract

[ABSTRACT]

[MEANS FOR SOLUTION] A tuning circuit having an amplitude-varying function is disclosed that comprises a coil, a capacitor, and a resistance-adjusting element connected in parallel to the coil and the capacitor for varying resistance at time of resonance of the tuning circuit, wherein the amplitude of an output signal of the tuning circuit is varied by varying the resistance with the resistance-adjusting element.

[SELECTED DRAWING] Fig. 3